**OBTAINING A RELIABLE SETTLING-TIME MEASUREMENT IS DIFFICULT AND REQUIRES A CAREFUL APPROACH AND AN EXPERIMENTAL TECHNIQUE. YOU CAN USE NEW CIRCUITS TO TEST THE 30-NSEC SETTLING TIME OF A PRECISION WIDEBAND AMPLIFIER.**

# Measuring precision-amplifier settling time

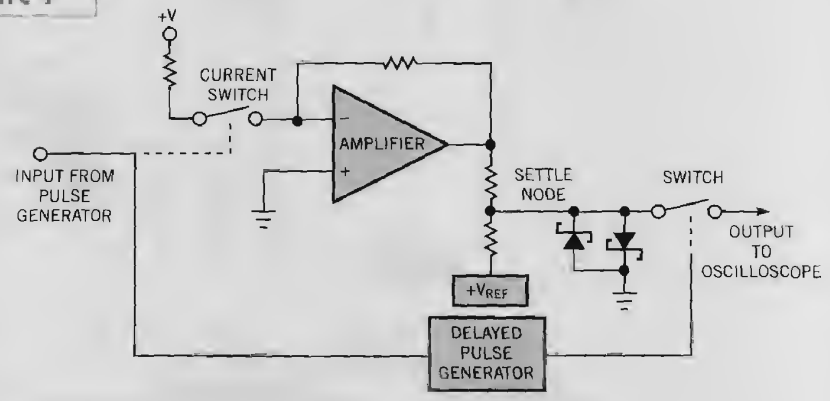
COUNTLESS APPLICATIONS, INCLUDING instrumentation, waveform-generation, and data-acquisition systems, use wideband amplifiers. Some of the new amplifiers combine precision with high-speed operation. As with many other components, the dc specifications are relatively easy to verify. However, ac specifications and settling time require sophisticated measurement approaches. Obtaining a reliable nanosecond-region settling-time measurement is difficult and requires a careful approach and an experimental technique.

A previous article discussed the basics of settling-time measurements and the techniques for measuring the settling time of a 16-bit DAC together with its output amplifier (**Reference 1**). The techniques necessary to measure the settling time of an amplifier by itself are similar but have significant differences. For one, the circuit to measure only the amplifier settling time is 60 times faster than the 16-bit DAC measurement circuit. Also, the measurement is less precise: 0.1% versus 0.0015%.

High-speed settling time is difficult to measure because the most common circuit for measuring settling time, which uses the "false-sum-node" technique, suffers from many drawbacks. The circuit requires the input pulse to have a flat top within the required measurement limits, which are typically settling within 5 mV or less for a 5V step. No general-purpose pulse generator can hold output amplitude and noise within these limits. The generator's output causes aberrations to appear at the oscilloscope probe, and these aberrations are indistinguishable from amplifier-output movement. Thus, the results are unreliable.

The oscilloscope connection also presents problems. As probe capacitance rises, ac loading of the circuit's resistor junction influences observed set-

Figure 1




**The switch at the input gates a current step to the amplifier under test, making the circuit insensitive to pulse-generator aberrations. The output, or sampling, switch prevents the oscilloscope from monitoring the settle node until settling is nearly complete, thereby eliminating overdrive.**

tling waveforms. A 10-pF probe alleviates this problem, but this probe's 10× attenuation sacrifices oscilloscope gain; 1× probes are unsuitable because of their excessive input capacitance.

Finally, the 400-mV drop across the clamp diodes at the circuit's settle node can cause the oscilloscope to undergo an unacceptable overload, which brings the displayed results into question because the overdrive-recovery characteristics of oscilloscopes can vary widely.

Thus, measuring an amplifier's settling time requires a "flat-top" pulse generator and an oscilloscope that is somehow immune to overdrive. These issues are central to a wideband-amplifier settling-time measurement.

## SWITCH CURRENT, NOT VOLTAGE

You can avoid the flat-top pulse-generator requirement by switching current rather than voltage. It is easier to gate a quickly settling current into the amplifier's summing node than to control a voltage. This approach makes the input-pulse generator's job easier, although it still must have a rise time of 1 nsec or less to avoid measurement errors (see **sidebar** "Subnanosecond-rise-time pulse generators for the rich and poor").

The only oscilloscope technology that offers inherent overdrive immunity is the classic sampling scope, which you should not confuse with modern DSOs that have overdrive restrictions. Unfortunately, manufacturers no longer make these instruments, although some are still available on the secondary market. You can, however, construct a circuit that borrows the overload advantages of classic sampling-oscilloscope technology. Also, the circuit can include features for measuring settling times of around 1 nsec.

## MEASURE NANOSECOND-REGION SETTLING

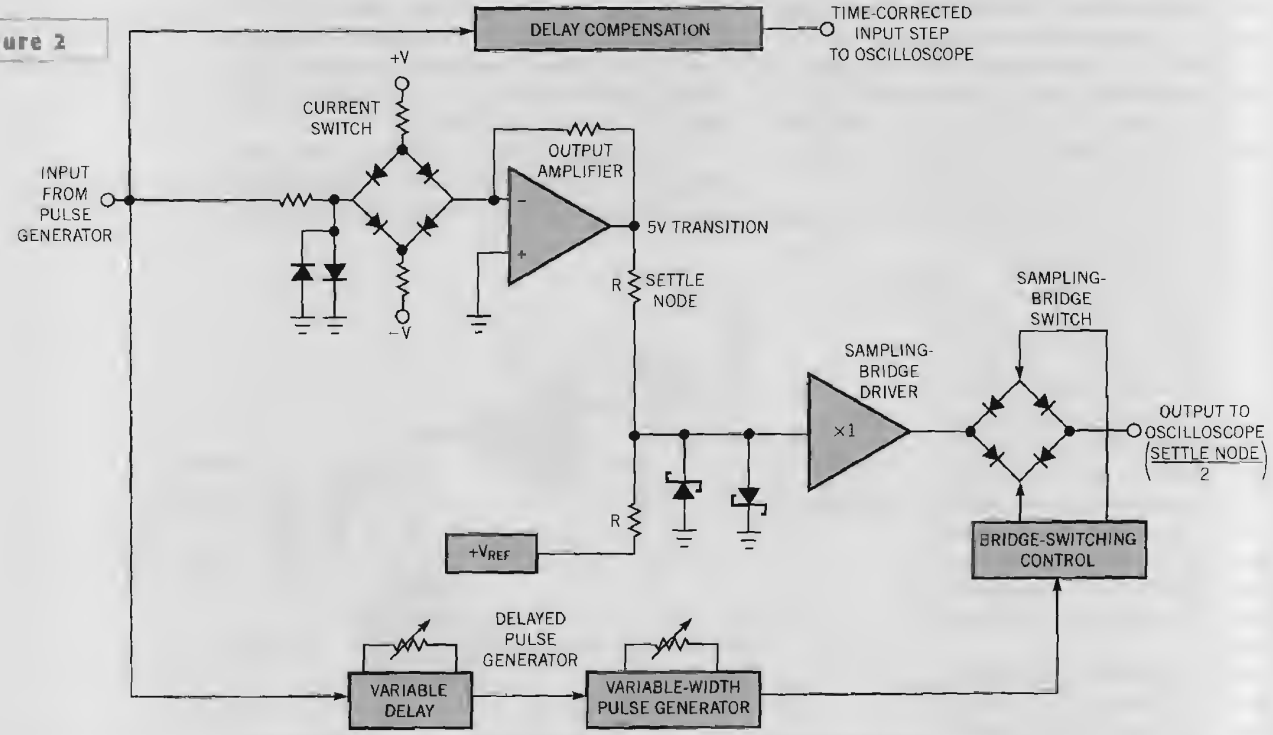
**Figure 1** is a conceptual diagram of a settling-time measurement circuit. This **figure** shares attributes with the false-sum-node circuit but has some additional features. The oscilloscope connects to the settle point through a switch, and the input pulse triggers a delayed pulse generator that determines the switch's state. The circuit sets the timing of the delayed pulse generator so that the switch does not close until settling is nearly complete. In this way, the circuit samples the time as well as the amplitude of the incoming waveform. The circuit never subjects the oscilloscope to overdrive, and no off-screen activity ever occurs. The oscilloscope displays only the tail end of amplifier settling.

The input pulse controls a switch at the amplifier's summing junction. This switch gates current to the amplifier through a voltage-driven resistor and eliminates the flat-top pulse-generator requirement, although the switch must be fast and devoid of drive artifacts.

**Figure 2** provides a more complete representation of the settling-time-measurement scheme. The delayed pulse generator now comprises a delay and a pulse generator, both independently variable. The input step to the oscilloscope undergoes delay compensation, which compensates for the propagation delay of the measurement path.

The most striking new aspects of the diagram are the diode-bridge switches. Borrowed from classic sampling-oscilloscope circuitry, these switches are key to the measurement. The inherent balance of a diode bridge eliminates charge-injection-based errors, and a diode bridge

Figure 2

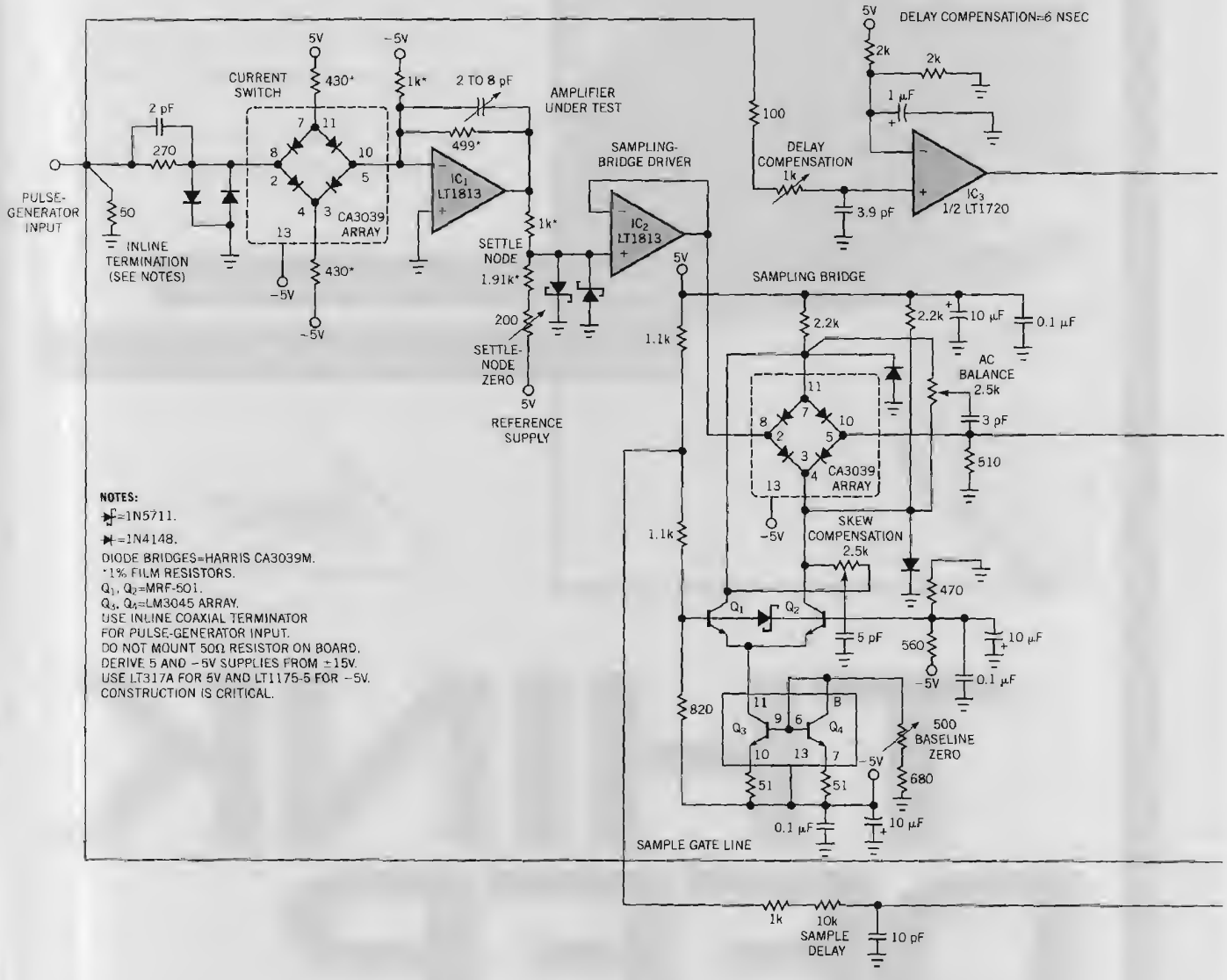



**Using diode bridges for the current and sampling-bridge switches eliminates charge-injection-based errors. Each bridge's balance, combined with matched, low-capacitance monolithic diodes and high-speed switching, yields clean switching.**

is superior to other electronic switches in this characteristic. Any other high-speed-switch technology contributes excessive output spikes due to charge-based feedthrough. FET switches are unsuitable because their gate-channel capacitance permits such feedthrough. This capacitance allows gate-drive artifacts to corrupt switching, defeating the switches' purpose.

The diode-bridge balance, combined with matched, low-capacitance monolithic diodes and high-speed switching, yields clean switching. The input-driven bridge quickly switches current into the amplifier's summing point, and settling occurs within a few nanoseconds. The diode clamp to ground at this bridge's input prevents excessive bridge-drive swings and ensures that input-pulse characteristics are irrelevant. The output, or sampling, bridge requires considerable attention to achieve the desired performance. The monolithic bridge diodes tend to cancel each other's temperature coefficient—drift is only about 100 μV/°C, but a dc balance is necessary to minimize offset. Trimming the bridge's on-current for zero I/O offset voltage provides dc balance. An ac-balance trim is necessary to correct for diode and layout capacitive imbalances, and a skew-compensation trim corrects for any timing asymmetry in the nominally complementary bridge drive. These ac

Figure 3

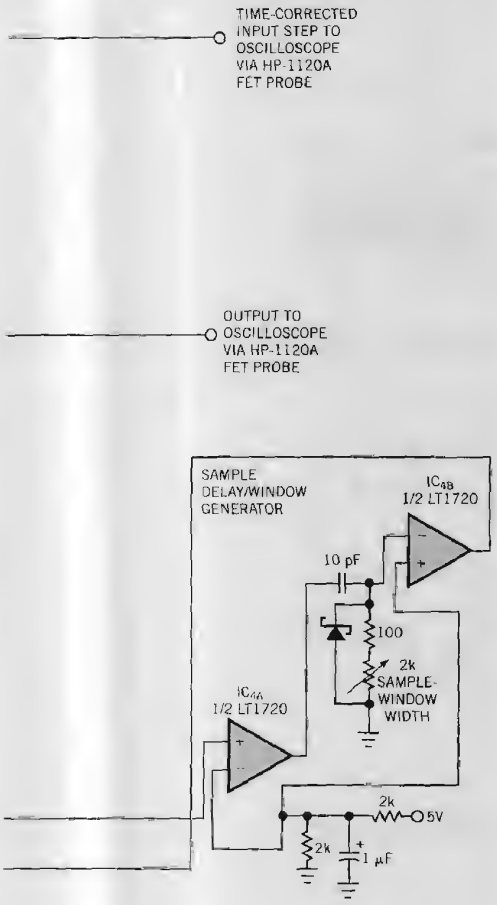



**This settling-time-measurement circuit closely follows the block diagram of Figure 2. Optimum performance requires attention to layout.**

trims compensate small dynamic imbalances, minimizing parasitic bridge outputs.

### DETAILED SETTLING-TIME CIRCUITRY

**Figure 3** details the settling-time measurement circuitry for $IC_1$, the LT1813 amplifier under test. The input pulse switches the input bridge and also routes to the oscilloscope via a delay-compensation network. The delay network, comprising a fast comparator, $IC_3$,



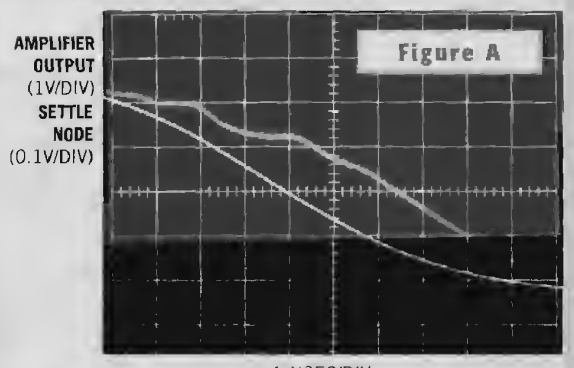

## MEASURING AND COMPENSATING SETTLING-CIRCUIT DELAY

The settling-time-measurement circuit uses an adjustable delay network to time-correct the input pulse for delays in the signal-processing path. Typically, these delays introduce errors of 20%, so an accurate correction is necessary. Setting the delay-compensation potentiometer involves observing the network's I/O delay and adjusting for the appropriate time interval. Determining the "appropriate" time interval is somewhat more complex and requires a wideband oscilloscope with FET probes. To ensure accuracy in the following delay measurements, you must verify the probe's time skew. Connect the probes to a subnanosecond pulse generator and verify the probe skew within 100 psec. Verifying the probe skew ensures small error for the delay measurements, which will be approximately 1 nsec.

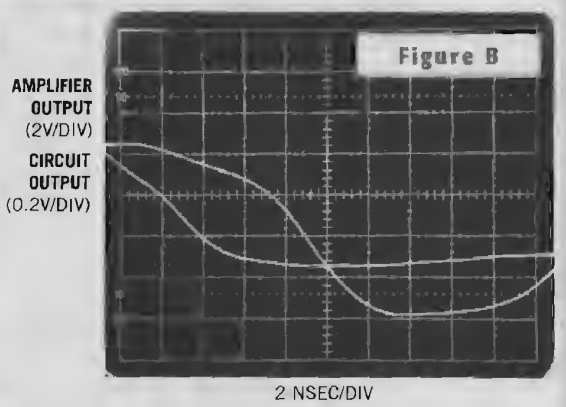
For the settling-time-measurement circuit, three delay measurements are of interest: the delay from the pulse generator to the amplifier under test, the delay from the amplifier under test to the settle node, and the delay from the amplifier under test to the output.

The delay from the pulse-generator input to the amplifier under test is approximately 800 psec. **Figure A** indicates 2.5 nsec from the amplifier under test to the settle node. **Figure B** indicates 5.2 nsec from the amplifier under test to the output. In **Figure A**'s measurement, the probes have a severe source-impedance mismatch. You can compensate for this mismatch by adding a series 500Ω resistor to the probe that monitors the amplifier under test. This provision approximately equalizes this probe's source impedance and negates the probe's input-capacitance term, which is approximately equal to 1 pF.

The measurements reveal a circuit I/O delay of 6 nsec, and you apply this correction by adjusting the 1-kΩ delay-compensation trim at the input to $IC_3$ in the settling-time-measurement circuit.




**The delay from the amplifier-under-test output to the settle node is 2.5 nsec.**




**The delay from the amplifier-under-test output to the circuit's output is 5.2 nsec.**

and an adjustable RC network, compensates the oscilloscope's input step signal for the 6-nsec delay through the circuit's measurement path (see **sidebar** "Measuring and compensating settling-circuit delay"). The circuit compares $IC_1$'s output to the 5V reference via the summing resistors at the settle node. The 5V reference also furnishes the bridge's input current, making the measurement ratiometric. The −5V-reference supply pulls current from the summing point at $IC_1$'s inverting input, allowing the amplifier a 5V step from +2.5V to −2.5V. $IC_2$ unloads the clamped settle node and drives the sampling bridge.

The input pulse triggers the $IC_4$-based delayed pulse generator. This circuitry produces a delayed pulse whose width sets the on-time of the sampling bridge. The 10-kΩ sample-delay potentiometer controls delay time, and the 2-kΩ sample-window-width potentiometer controls pulse width. If you appropriately set the delay, the circuit provides no input to the oscilloscope until settling is nearly complete, eliminating overdrive. You adjust the sample-window width so that all remaining settling activity is observable. In this way, the oscilloscope's output is reliable, and you can take meaningful data. $Q_1$ through $Q_4$ level-shift the output of the delay generator to provide complementary switching drive to the bridge. The actual switching transistors, $Q_1$ and $Q_2$, are UHF types, permitting true differential bridge switching with less than 1 nsec of time skew.

**Figure 4** shows circuit waveforms.

## SUBNANOSECOND-RISE-TIME PULSE GENERATORS FOR THE RICH AND POOR

The input diode bridge of the settling-time measurement circuit requires a subnanosecond-rise-time pulse to cleanly switch current to the amplifier under test. The ranks of pulse generators providing this capability are thin. Instruments with rise times of 1 nsec or less are rare, and costs are excessive. Current-production units can easily cost $10,000, and prices rise to-

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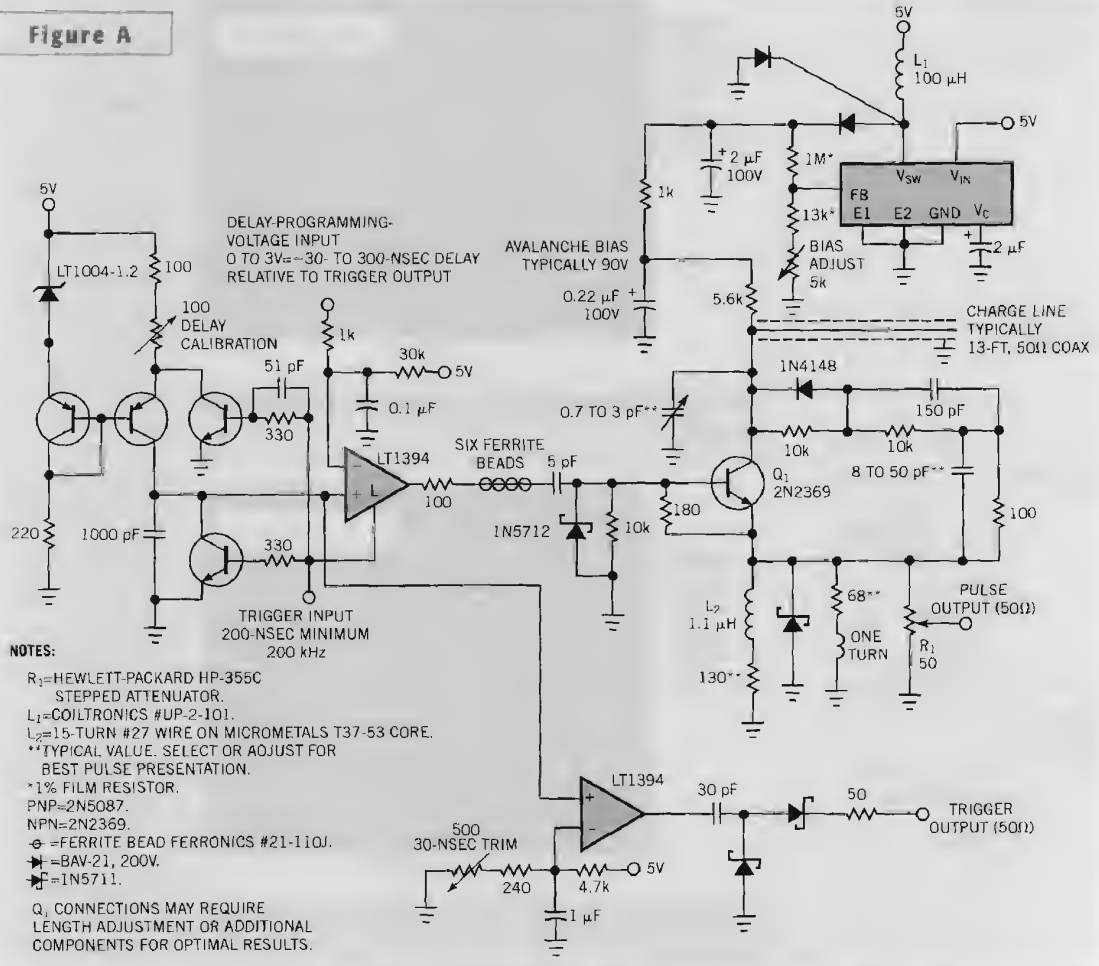
Figure A




**A programmable delay triggers this subnanosecond-rise-time pulse generator. The charge line at $Q_1$'s collector results in a 40-nsec output width.**

ward $30,000 depending on features. Substantially less expensive approaches are available for bench work and production testing.

The secondary market offers subnanosecond-rise-time pulse generators at attractive cost. The Hewlett-Packard HP-8082A transitions in less than 1 nsec, has a full complement of controls, and costs about $500. The HP-215A, long out of manufacture, has 800-psec edge times and is a clear bargain with a typical price lower than $50. This instrument also has a versatile trigger output, which permits continuous-time phase adjustment from before to after the main output. External trigger impedance, polarity, and sensitivity are also variable. The output, controlled by a stepped attenuator, puts 610V into 50Ω in 800 psec.

The Tektronix type 109 switches in 250 psec. Although amplitude is fully variable, charge lines are necessary to set pulse width. This reed-relay-based instrument has a fixed repetition rate of approximately 500 Hz and no external trigger facility, making it somewhat unwieldy to use. Price is typically $20. The Tektronix type 111 is more practical. Edge times are 500 psec, and the device has fully variable repetition rate and external trigger capabilities. The charge-line length sets the pulse width. Price is usually about $25.

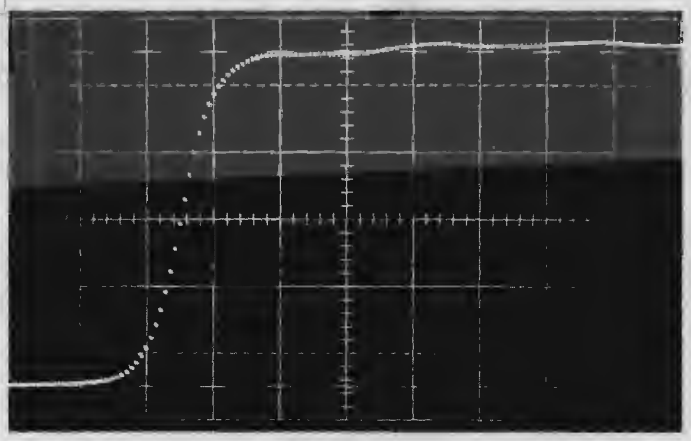
A potential problem with older instruments is availability. Residents of Silicon Valley tend toward inbred techno-provincialism. Citizens of other locales cannot simply go to a flea market, junk store, or garage sale and buy a subnanosecond pulse generator. **Figure A** shows a circuit that produces subnanosecond-rise-time pulses. The circuit's operation essentially duplicates the Tektronix type 111 pulse generator. Rise time is 500 psec, and pulse amplitude is fully adjustable. An external input determines repetition rate, and you can set the occurrence of the output pulse from before to after a trigger output.

This circuit uses an avalanche pulse generator, $Q_1$, to create extremely fast rise-time pulses. The transmission-line length at $Q_1$'s collector sets the pulse width, and a coaxial-cable charge line attaches to the collector. In this case, a 13-ft charge line produces a 40-nsec-wide output.

The picture in **Figure B**, taken with a 3.9-GHz bandpass oscilloscope (Tektronix 547 with 1S2 sampling plug-in) shows output-pulse purity and rise time. The rise time is 500 psec with minimal preshoot and pulse-top aberrations. The pulse's falling edge has similar characteristics.

This level of cleanliness requires considerable layout experimentation, particularly with $Q_1$'s emitter and collector lead lengths and associated components. Ground-plane-type construction with high-speed layout, connection, and termination techniques is essential for good results from this circuit. Additionally, small inductances or RC networks may be necessary between $Q_1$'s emitter and $R_1$ to get best pulse presentation.

Figure B




**The pulse-generator output shows a 500-psec rise time with minimal pulse-top aberrations.**

Trace A is the time-corrected input pulse, Trace B is the amplifier output, Trace C is the sample gate, and Trace D is the settling-time output. When the sample gate goes low (Trace C), the bridge switches cleanly, and the last 10 mV of slew is easily observable. Ring time is also clearly visible, and the amplifier settles nicely to final value. When the sample gate goes high, the bridge switches off with only millivolts of feedthrough. Note that no off-screen activity occurs; the oscilloscope is never subjected to overdrive.

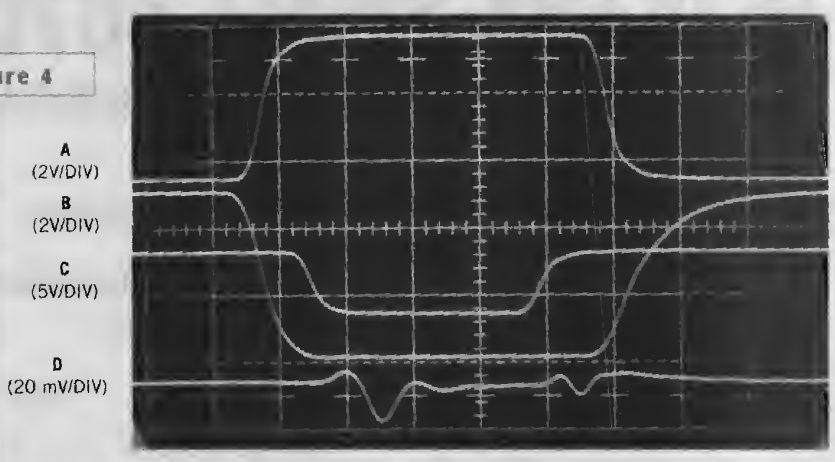
**Figure 5** expands vertical and horizontal scales so that settling detail is more visible. Note that this photo measures settling time from the onset of the time-corrected input pulse. Appropriate setting of the oscilloscope gain results in an amplitude measurement with respect to the amplifier, not the sampling bridge's output. This calibration eliminates the ambiguity that the ÷2 ratio of the summing resistors at the settle node introduces. Trace A is the time-corrected input pulse, and Trace B is the settling output. The last 20 mV of movement, which begins at the center-screen vertical marker, is easily observable, and the amplifier settles inside 5 mV (0.1%) in 30 nsec after the onset of the input step.

## PROPERLY SET TRIMS

As mentioned, the circuit requires dc and ac trimming to achieve this level of performance. Making these adjustments requires disabling the amplifier by disconnecting the input-current switch and

the 1-kΩ resistor at the amplifier and shorting the settle node directly to the ground plane (**Reference 2**). With the amplifier disabled and the settle node grounded, the output should theoretically always be zero, but this is not the case for an untrimmed bridge. Because the sample gate's transitions cause large signal swings, ac and dc errors are present. Additionally, the output shows significant dc-offset error during the sampling interval. Adjusting the ac-balance and skew-compensation trims minimizes the switching-induced transients. The baseline-zero trim adjusts the dc offset. Using these adjustments, you can minimize all switching-related activity and reduce offset error to unreadable levels. You can use the settle-node-zero trim to correct for any further differences between the presettling and postsettling baseline.

Figure 4

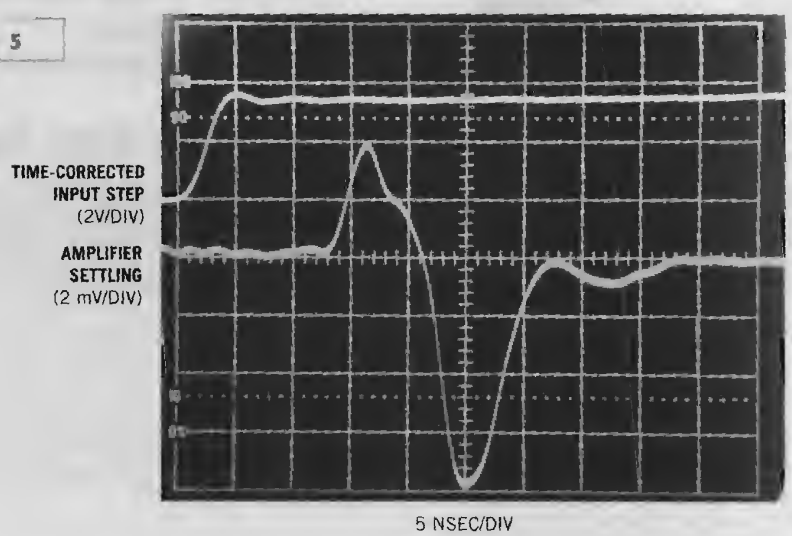



**Settling-time-circuit waveforms include the time-corrected input pulse (Trace A), the amplifier-under-test output (Trace B), the sample gate (Trace C), and the settling-time output (Trace D).**

Some other factors are important for the circuit to operate properly (**Reference 2**). First, you must properly position the sampling window in time. Initiating the sample window too early causes the measurement circuit's output to overdrive the oscilloscope when sampling commences. In general, it's good practice to "walk" the sampling window up to the last 10 mV or so of amplifier slewing so that the onset of ring time is observable. Second, the amplifier requires frequency compensation using the $C_{COMP}$ capacitor in **Figure 3** to get the best possible settling time. Light compensation permits fast slewing but causes excessive ringing amplitude over a long time. At the other extreme, a large value for $C_{COMP}$ eliminates all ringing but slows the amplifier so that settling stretches to 50 nsec. A carefully chosen capacitor value results in tightly controlled damping and a settling time of 30 nsec.

Finally, achieving this level of performance depends on layout. The circuit's construction involves a number of subtleties and is crucial.□

Figure 5




**Expanded vertical and horizontal scales show 30-nsec amplifier settling time to within 5 mV.**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AUTHOR'S BIOGRAPHY

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